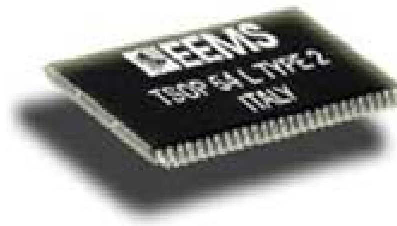
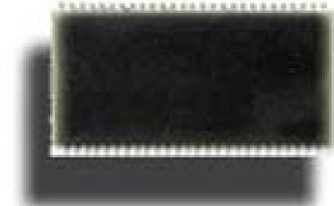
TSOP II

Thin Small Outline Package Type II





EEMS offers TSOP II package, developped to accommodate devices having the pads at the center of the die: almost all DRAM are designed for a center bond package. Such specific geometry requires the active side of the die is attached to the back of the leadframe: Lead On Chip technology.

EEMS produces high volume of this small and thin package (1.0 mm body thickness), using the Thermoplastic LOC assembly technology and offering a "Full Test Flow", including Burn-In, performed on a large set of "State od the Art" memory testers, suitable for the very high frequency of the last DDR memory generation and above.

In addition, EEMS offers on some dedicated SMT lines the assembly of packaged memory into full tested DIMM Modules, directly pluggable in the end equipment.

The TSOP II packages are available in various pin count and are automatically fully inspected to insure flatness and coplanarity.

Features & Benefits

- Small board area needed
- Small size
- Cost competitive
- High reliability
- Thermoplastic Lead On Chip tecnology
- Compliant to Rohs directive 2002/95/CE

Applications

Memory, memory and memory are the primary users of this package.

Device

- SDRAM
- DRAM
- DDR
- All Center Bond Memory
- DIMM
- SIMM

End Equipment

- Desktop and Notebook PCs
- Memory Modules
- Telecom Systems
- Industrial Systems
- PC Expansion Cards

Standard Materials

Substrate	AL42 Leadframe
Die Attach	LOC Tape
Gold wire	24-30 um
Mold Compound	Epoxy
Lead Solder Plating	85/15 Sn/Pb or 100% Sn
Packing	Jedec Tray/Tape & Reel
Packing option	Dry Pack

Process Highlights

Processable wafer	200 – 300 mm
Die Tickness	0.280 mm max
Bond Pad Pitch	60 um min
Marking	Laser
Lead inspection	Auto inspection

EEMS

TSOP II

Specifications

Electrical (simulated w/bondwire)

(10.16 x 22.22 x 1.0 mm body with 66 leads)

Capacitance (pF) : 1.0 - 1.6 at 1 GHz

Inductance (nH) : 2.7 - 5.3 at 1 GHz

Resistance (mΩ) : 130 - 270 at 100 Mhz

Thermal Resistance (simulated)

(12 x 18.4 x 1.0 mm with 48 leads; 1 Watt, 0 m/s airflow as per JEDEC JESD51.2):

Θ ja = 34 ºC/watt Typical

Reliability

Moisture Sensitivity : JEDEC MSL 1 @ up to 260 ºC,

High Temp Storage : 150 ºC, 1000 hours

Temp Cycle : -65/+150 ºC, 1000 cicles

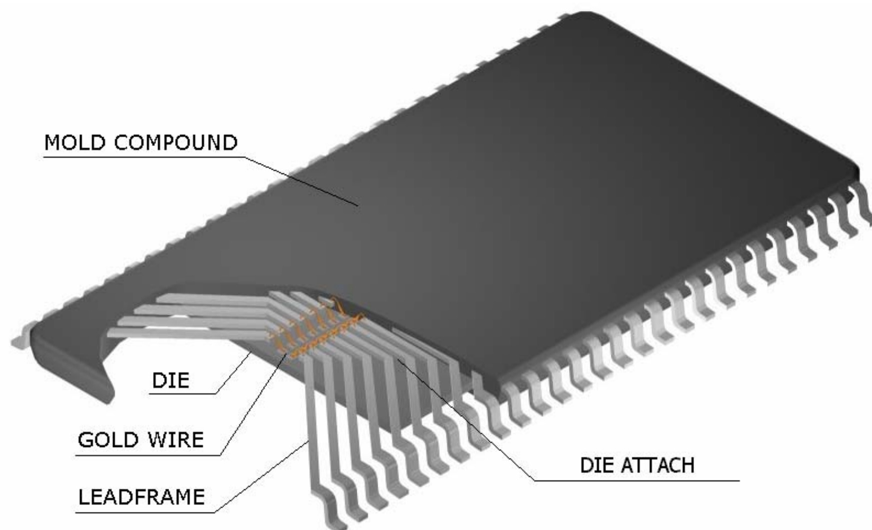
Temp Humidity Test : 130 ºC/85% RH, 240 hours HAST

PCT : 121 ºC/2 atm., 240 hours

Available Services

- 300 mm wafer full processing
- Wafer backgrinding
- Wafer map / sort
- Product Engineering
- -30 + 125 ºC full test
- Dynamic Burn In
- Compliant to Rohs directive 2002/95/CE
- Modules (DIMM) Assembly & Test

Cross – Section



TSOP II Nominal Package Dimensions (mm)

Body Area	Lead Count	Lead Pitch	Lead edge to edge	Body Thickness	Stand-off	Overall Height	JEDEC
10.16 x 22.22	86	0.50	11.76	1.00	0.10	1.2 max	MS-024 FB
10.16 x 22.22	66	0.65	11.76	1.00	0.10	1.2 max	MS-024 FC
10.16 x 22.22	54	0.80	11.76	1.00	0.10	1.2 max	MS-024 FA

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