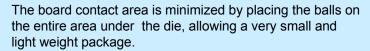
FBGA

Fine pitch Ball Grid Array

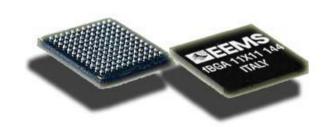
EEMS offers the FBGA as a near Chip Size Package, based on a BT laminate substrate with a Ball Grid Array format.

The assembly technology is gold wire and molding on the PCB with solder balls for board contact.



Body sizes and ball counts are designed to fit the specific customers needs (the two Tables show the range of the FBGA capabilities and the packages in production).

These packages are also well suited to products requiring low inductance as the PCB design can take this requirement into account and be designed accordingly.



Features & Benefits

- · Small board area needed
- Small size
- Cost competitive
- High reliability
- Compliant to Rohs directive 2002/95/CE
- · Die Stack capability

Applications

DSP's ASIC's RF Devices

Anywhere a smaller footprint is required, an FBGA should be used.

These packages are smaller than conventional BGA's and also comparable with leadframe packages.

eadframe packages. Device End Equipment SRAM Portable PC's Flash Hard Disk Drivers PC Graphics

•	r C Grapines						
•	Mobile phones						
•	PDA's						

FBGA Capabilities									
Item	Min. Max.		Notes						
Foot Print (mm)	5 x 5	17 x 17	All dimensions in increment of 0.1 mm, quad and rectangular						
Thickness (mm)	1.00	1.70	All dimensions in increment of 0.1 mm						
Ball Dia (um)	300	500	All dimensions in increment of 50 um						
Ball Arrays	5 x 5	21 x 21	Full matrix and depopulated						
Ball Pitches (mm)	0.5	1.0	0.65, 0.75, 0.80 mm also available						

Standard Materials

Substrate BT or equivalent
Die Attach Low stress mtl
Gold wire 24 - 30 um
Mold Compound Epoxy

Solder Ball Eutectic 63/37 or Sn/4.0Ag/0.5Cu alloy

Jedec Tray/Tape & Reel

Packing option Dry Pack

Process Highlights

Processable wafer 200 – 300 mm
Die Tickness 0.300 mm max
Bond Pad Pitch 60 um min
Marking Laser

Ball inspection Auto inspection



Packing

FBGA

Specifications

Electrical (simulated w/bondwire)

(11 x 11 mm body with 144 balls)

Capacitance (pF) : 0.34 – 0.75 at 1.5 GHz

Inductance (nH) : 2.0 - 3.4 at 1.5 GHz

Resistance (m Ω) : 310 – 770 at 1.5 Ghz

Thermal Resistance (simulated)

(11x11 mm body with 144 balls; 4 layers PCB and 1 Watt, 0 m/s airflow as per JEDEC JESD51.2):

Θ ja = 25 °C/watt Typical

Reliability

Moisture Sensitivity : JEDEC MSL 3 @ up to 260 °C,

High Temp Storage : 150 °C, 1000 hours

Temp Cycle : -55/+125 °C, 1000 cicles

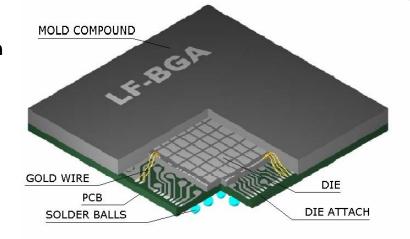
Temp Humidity Test : 130 °C /85% RH, 96 hours HAST

PCT : 121 °C/2 atm., 240 hours

Available Services

- PCB Design and simulation
- 300 mm wafer full processing
- · Wafer backgrinding
- Wafer map / sort
- Product Engineering
- -30 + 125 °C full test
- · Dynamic Burn In
- Compliant to Rohs directive 2002/95/CE

Cross - Section



FBGA Packages in production: Nominal Dimensions (mm)												
ID Letter	Body Size	Ball Count	Ball Pitch	Ball Matrix	Ball Diameter	PCB Thickness	Mold Cap Thickness	Total Thickness				
L-FBGA	11 x 11	144	0.80	12 x 12	0.48	0.31	0.77	1.7 max				
T-FBGA	8 x 10	48	0.75	6 x 8	0.40	0.26	0.52	1.2 max				
T-FBGA	6.4 x 6.4	46	0.75	6 x 8	0.40	0.31	0.52	1.2 max				
V-FBGA	6 x 8	54	0.75	6 x 9	0.35	0.21	0.48	1.0 max				
V-FBGA	6 x 8	48	0.75	6 x 8	0.35	0.21	0.48	1.0 max				
V-FBGA	7.7 x 9	44	0.50	4 x 10 + 4	0.30	0.21	0.43	1.0 max				

