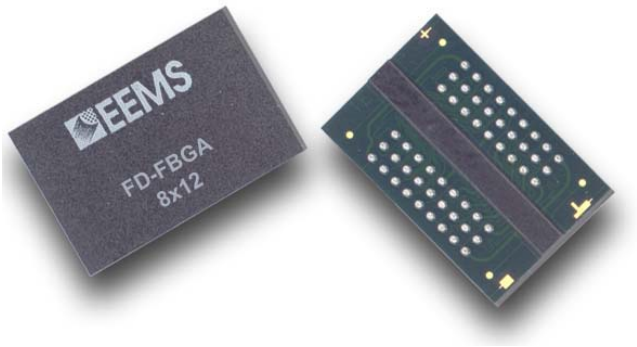
FD-FBGA

Face Down-Fine pitch BGA

EEMS offers the FD-FBGA as a near Chip Size Package, based on a BT laminate substrate with a Ball Grid Array format.

The FD-FBGA has been developped to accommodate devices with pads in the center of the die, like most of the DRAM are. Such specific geometry requires the active side of the die to face down on the substrate.



The assembly technology is gold wire and molding on the PCB with solder balls for board contact. The board contact area is minimized by placing the balls on the entire area under the die, allowing a very small and light weight package.

Body sizes and ball counts are designed to fit the specific customers needs (the two Tables show the range of the FD-FBGA capabilities and the already tooled packages).

These packages are also well suited to products requiring low inductance as the PCB design can take this requirement into account and be designed accordingly.

Features & Benefits

- Small board area needed
- Small size
- Cost competitive
- High reliability
- Compliant to Rohs directive 2002/95/CE
- Die Stack capability

Applications

High Speed Memory (Sdram, DDR, DDRII) and anywhere a Center Bond Device requires a smaller footprint, a FD-FBGA should be used.

Device

- SDRAM
- DRAM
- DDR
- All Center Bond Memory

End Equipment

- Portable PC's
- Desktop PC's
- Wireless Applications
- Mobile phones
- PDA's

FD-FBGA Capabilities

Item	Min.	Max.	Notes
Foot Print (mm)	5 x 5	17 x 17	All dimensions in increment of 0.1 mm, quad and rectangular
Thickness (mm)	1.00	1.70	All dimensions in increment of 0.1 mm
Ball Dia (um)	300	500	All dimensions in increment of 50 um
Ball Arrays	5 x 5	21 x 21	Full matrix and depopulated
Ball Pitches (mm)	0.5	1.0	0.65, 0.75, 0.80 mm also available

Standard Materials

Substrate	BT or equivalent
Die Attach	Low stress Tape
Gold wire	24 - 30 um
Mold Compound	Epoxy
Solder Ball	Eutectic 63/37 or Sn/4.0Ag/0.5Cu alloy
Packing	Jedec Tray/Tape & Reel
Packing option	Dry Pack

Process Highlights

Processable wafer	200 – 300 mm
Die Tickness	0.240 mm max
Bond Pad Pitch	50 um min
Marking	Laser
Ball inspection	Auto inspection

FD-FBGA

Specifications

Electrical (simulated w/bondwire)

(8 x 12 mm body with 60 balls)

Capacitance (pF) : 0.32 – 0.55 at 1.5 GHz

Inductance (nH) : 1.8 – 3.0 at 1.5 GHz

Resistance (mΩ) : 280 – 420 at 1.5 Ghz

Thermal Resistance (simulated)

(8 x 12 mm body with 60 balls; single layer PCB and 1 Watt, 0 m/s airflow as per JEDEC JESD51.2):

Θ ja = 32 °C/watt Typical

Reliability

Moisture Sensitivity : JEDEC MSL 3 @ up to 260 °C,

High Temp Storage : 150 °C, 1000 hours

Temp Cycle : -55/+125 °C, 1000 cicles

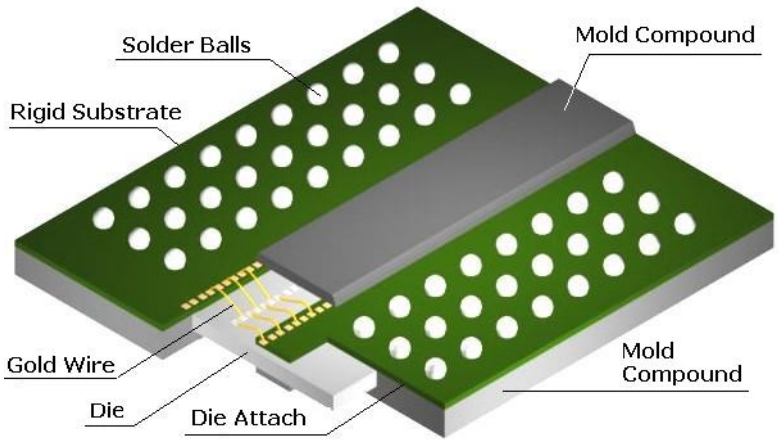
UHAST : 130 °C /85% RH, 240 hours

T & H : 85 °C/85% RH, 1000 hours

Available Services

- PCB Design and simulation
- 300 mm wafer full processing
- Wafer backgrinding
- Wafer map / sort
- Product Engineering
- -30 + 125 °C full test
- Dynamic Burn In
- Compliant to Rohs directive 2002/95/CE

Cross – Section



FD-FBGA Tooled Packages: Nominal Dimensions (mm)

ID Letter	Body Size	Ball Count	Ball Pitch	Ball Matrix	Ball Diameter	PCB Thickness	Mold Cap Thickness	Total Thickness
T-FBGA	8 x 12	54	0.80	9 x 9	0.40	0.29	0.56	1.2 max
T-FBGA	8 x 12	60	0.80 x 1.0	6 x 12	0.40	0.29	0.56	1.2 max
T-FBGA	8 x 12	60	0.80 x 1.0	6 x 12	0.45	0.29	0.56	1.2 max
T-FBGA	10 x 10.5	60	0.80	6 x 12	0.45	0.29	0.56	1.2 max
T-FBGA	10 x 12.5	84	0.80	6 x 15	0.45	0.29	0.56	1.2 max

EEMS